We Claim:

1. A printed circuit board comprising:

a first power plane;

a first ground reference plane including two opposite sides, wherein the first power plane is positioned proximate one side of the first ground reference plane; and

at least one signal layer, wherein the at least one signal layer is positioned proximate the other side of the first ground reference plane to isolate the first power plane from the at least one signal layer;

wherein any other signal layers in the printed circuit board are isolated from the first power plane by at least one ground reference plane.

2. The printed circuit board of Claim 1, wherein the first power plane and the first ground reference plane are positioned near the surface of the printed circuit board.

3. The printed circuit board of Claim 1, further comprising a second ground reference plane, wherein the first power plane is positioned among inner layers of the printed circuit board between the first and second ground reference planes.

4. The printed circuit board of Claim 1, further comprising a second ground reference plane and a second power plane, wherein:

the printed circuit board includes outer surfaces,

the first power plane and the first ground reference plane are positioned proximate a first outer surface of the printed circuit board,

the second power plane and the second ground reference plane are positioned proximate a second outer surface of the printed circuit board, and

the first signal layer is positioned between the first and second ground reference planes to isolate the first signal layer from the first and second power planes.

5. The printed circuit board of Claim 1, further comprising:

a first insulating layer positioned between the first ground reference plane and the first power plane;

a second insulating layer positioned between the first ground reference plane and the at least one signal layer.

6. The printed circuit board of Claim 1, further comprising an insulating layer positioned between the first ground reference plane and the first power plane, wherein the insulating layer is configured provides capacitance between the first ground reference plane and the first power plane.

7. The printed circuit board of Claim 1, wherein the first power plane includes at least two different subplanes configured to provide different voltages.

8. A method for stacking a multi-layer printed circuit board comprising:

isolating all power planes in the printed circuit board from all signal layers in the printed circuit board by positioning a ground plane between each group of one or more of thepower planes and each group of one or more of the signal layers.

9. The method of Claim 8, further comprising:

configuring the ground plane to provide a voltage reference for at least one of the signal layers.

10. The method of Claim 8, wherein the power planes, the ground planes, and the signal layers include conductive material, the method further comprising:

forming insulating layers between the layers that include conductive material.

11. The method of Claim 8, further comprising:

configuring the first power plane with a plurality of subplanes, wherein each subplane provides a different voltage.

12. The method of Claim 8, further comprising:

positioning the power planes proximate the middle layers of the printed circuit board.

13. The method of Claim 8, further comprising:

positioning the power planes proximate at least one outer layer of the printed circuit board.

14. The method of Claim 8, further comprising:

positioning a pads layer on the surface of the printed circuit board.

15. The method of Claim 8, further comprising:

positioning an integrated circuit on the pads layer.

16. An electronic system comprising:

a multi-layer printed circuit board including:

a plurality of power planes;

a plurality of signal layers; and

a plurality of ground planes, wherein at least one of the plurality of ground planes is positioned between each group of one or more of the plurality of power planes and each group of one or more of the signal layers to isolate each of the groups of one or more of the power planes from each of the groups of one or more of the signal layers.

17. The electronic system of Claim 16, wherein at least a portion of the plurality of signal layers include signal traces on a single side of a core layer.

18. The electronic system of Claim 16, wherein at least a portion of the plurality of signal layers include signal traces on two sides of a core layer.

19. The electronic system of Claim 16, further comprising:

an insulating layer positioned between each of the power planes, the ground plane, and the signal layers.

20. The electronic system of Claim 16, further comprising:
a ground plane positioned proximate each of the signal layers.

21. The electronic system of Claim 16, further comprising:
a pads layer positioned on at least one outer surface of the printed circuit board.

22. The electronic system of Claim 16, further comprising:
an integrated circuit mounted on the printed circuit board.

23. The electronic system of claim 16, wherein a plurality of power planes are positioned adjacent to a ground plane and separated by an insulating layer of thickness of approximately less than 1 mil.